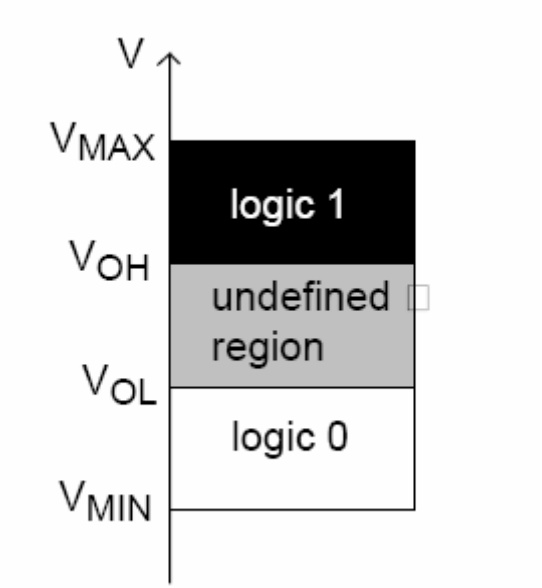
Lect. 20: Inverters (S&S 10.1-2)

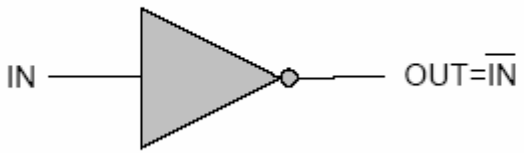
Digital Electronics



How to implement logic gates?

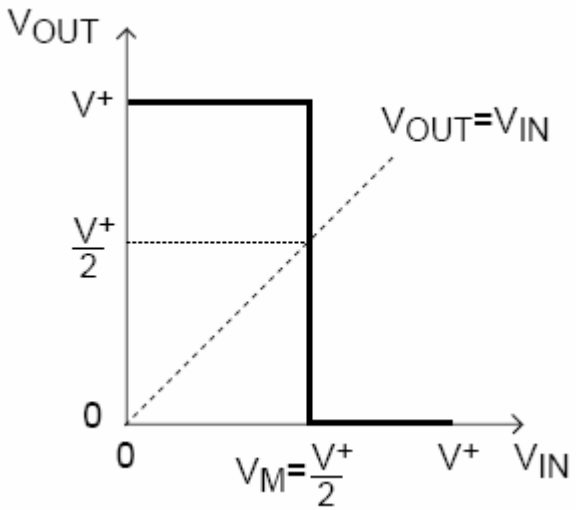
➔ Inverters are the basic building block!

Lect. 20: Inverters

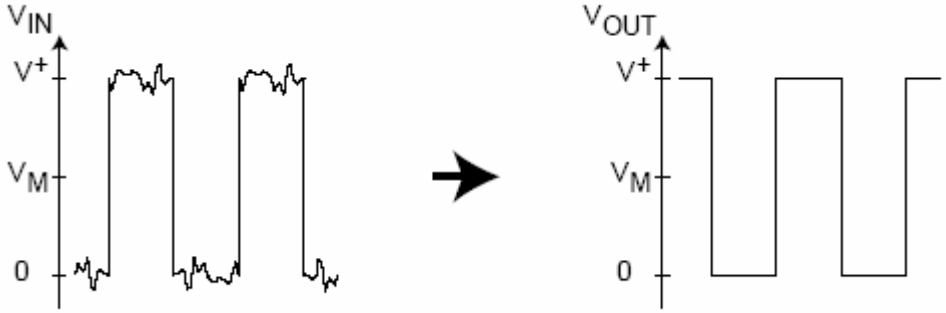


IN	OUT
0	1
1	0

Ideally,

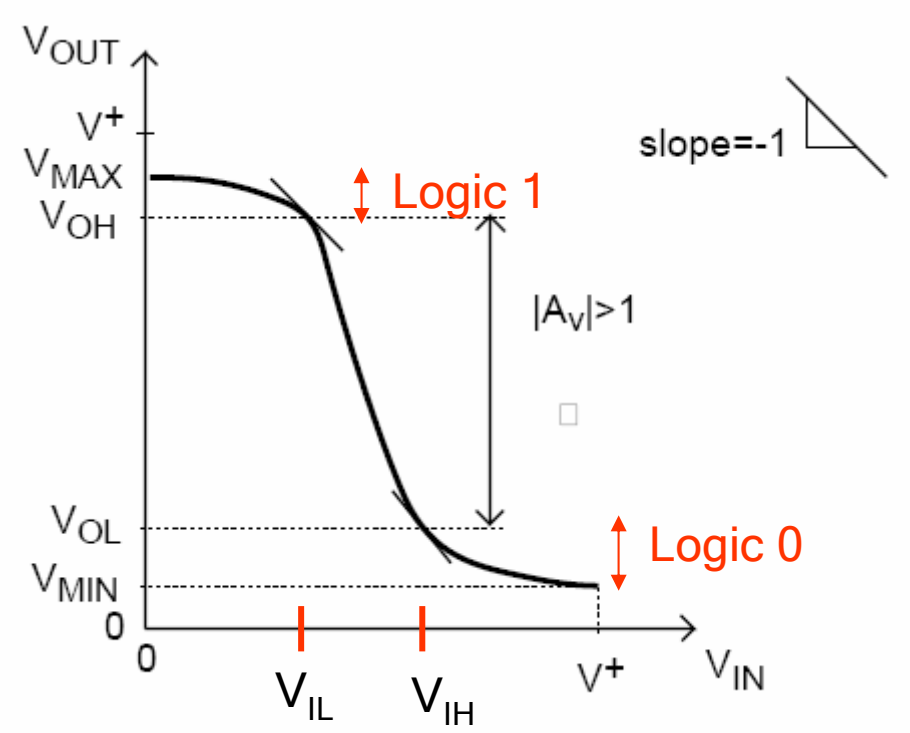


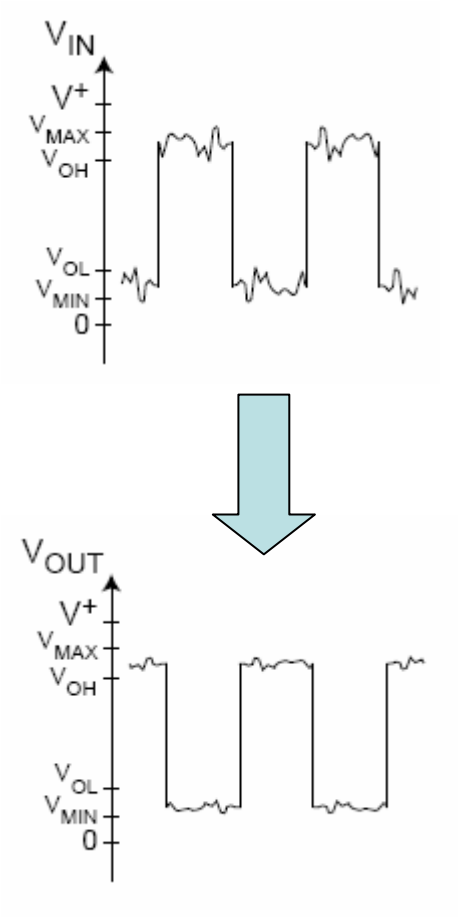
Signal can be regenerated



Lect. 20: Inverters

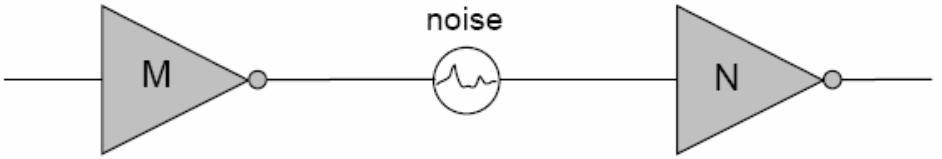
Real inverters

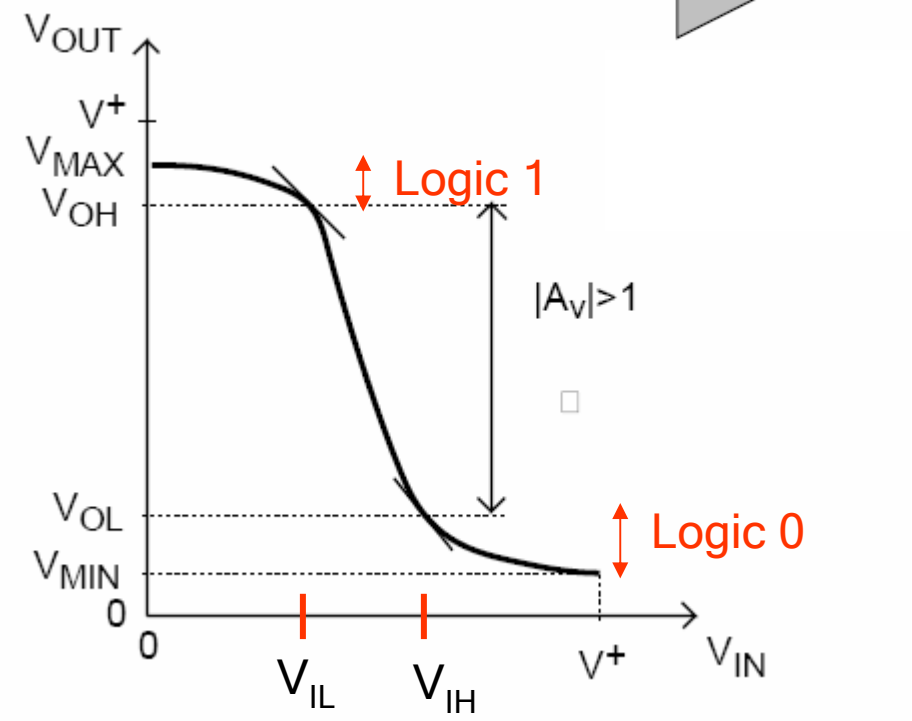


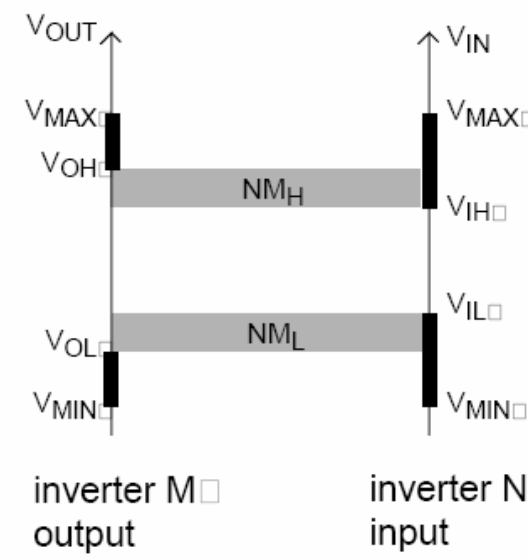


Lect. 20: Inverters

Noise Margin







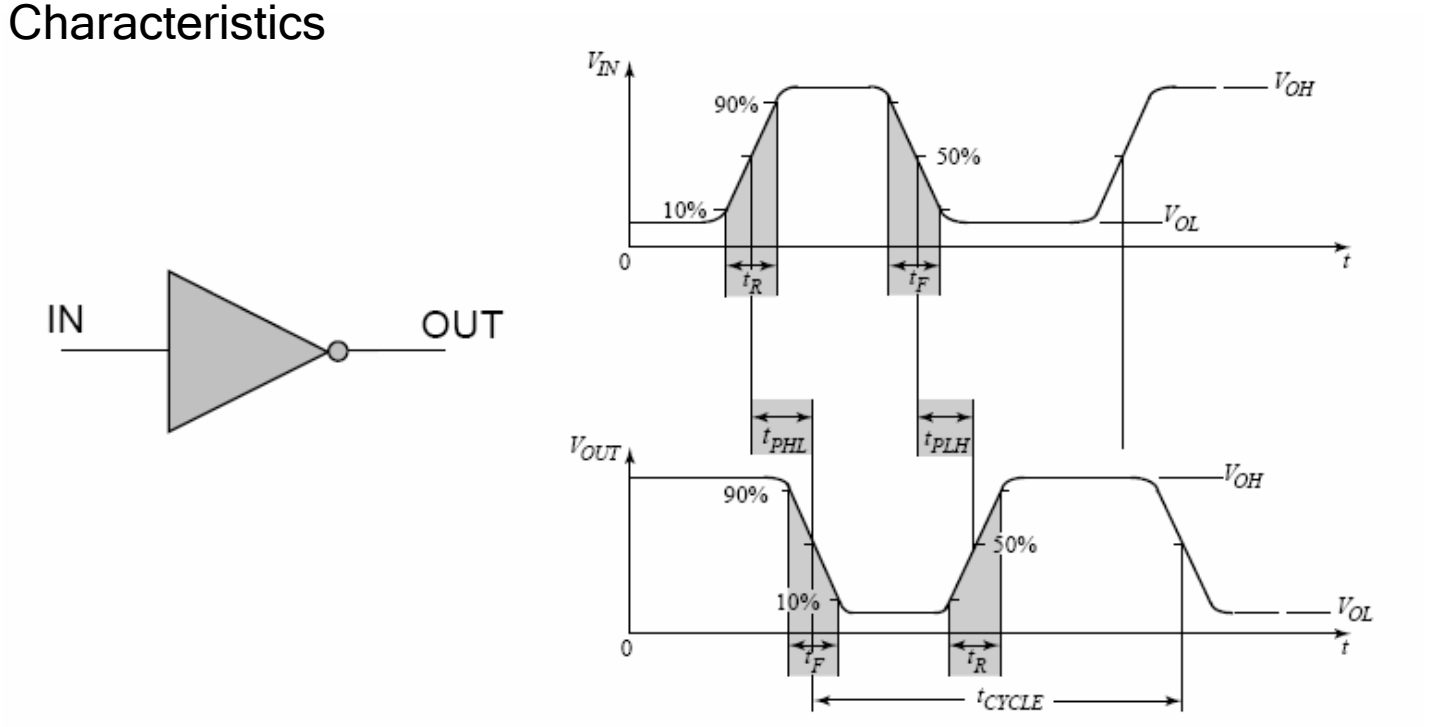
Larger noise margin
➔ smaller V_{IH}, larger V_{IL}

➔ Larger $|A_v|$

$$NM_H = V_{OH} - V_{IH}$$
$$NM_L = V_{IL} - V_{OL}$$

Lect. 20: Inverters

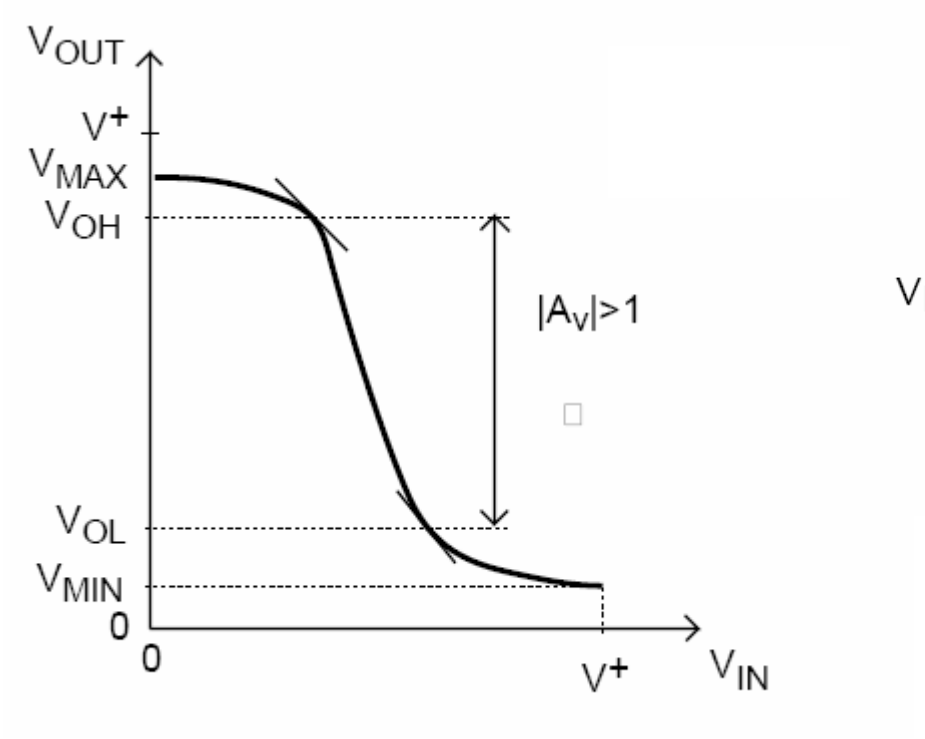
Transient Characteristics

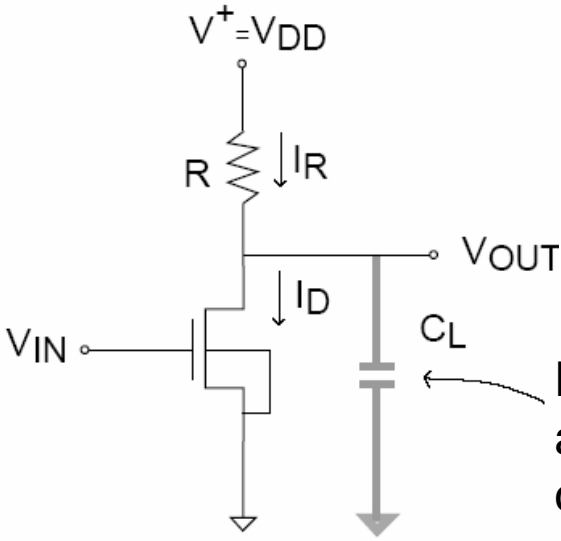


Propagation Delay: $t_P = \frac{1}{2}(t_{PHL} + t_{PLH})$

Lect. 20: Inverters

How to implement an inverter? CS amplifier configuration





Due to load as well as internal capacitance

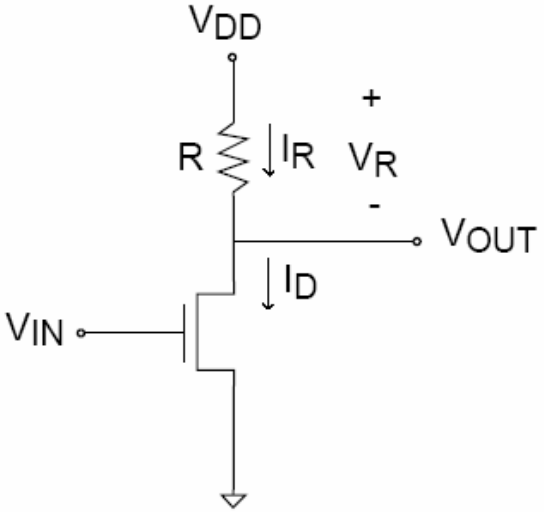
$V_{IN} < V_T$, MOSFET OFF $\Rightarrow V_{OUT} = V_{DD}$

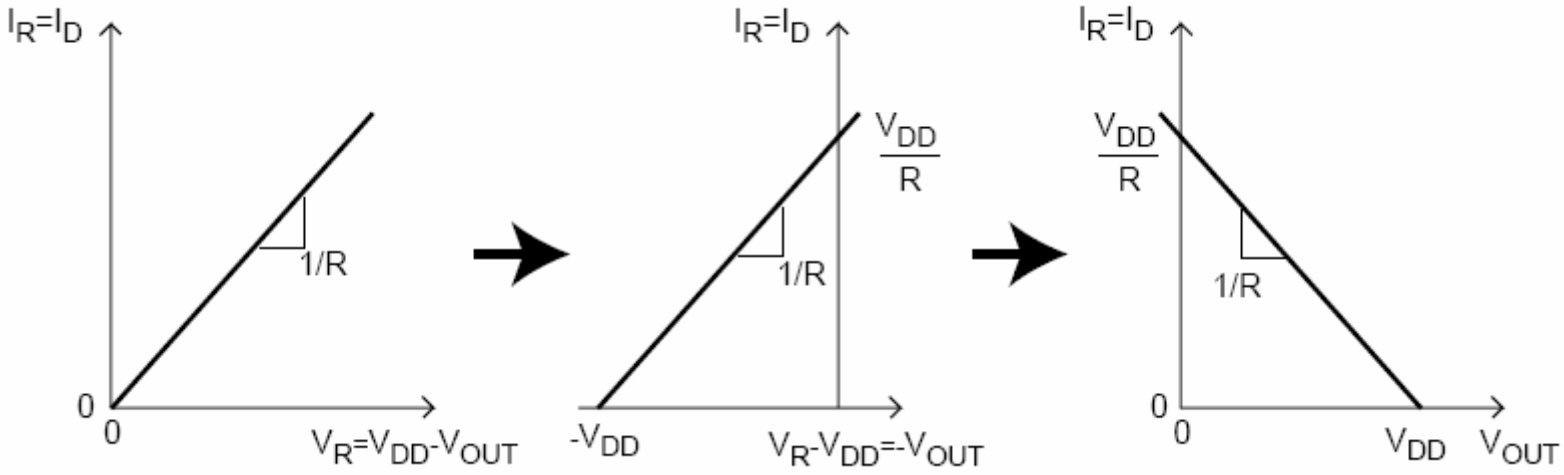
$V_{IN} > V_T$, MOSFET ON $\Rightarrow V_{OUT}$ small

Lect. 20: Inverters

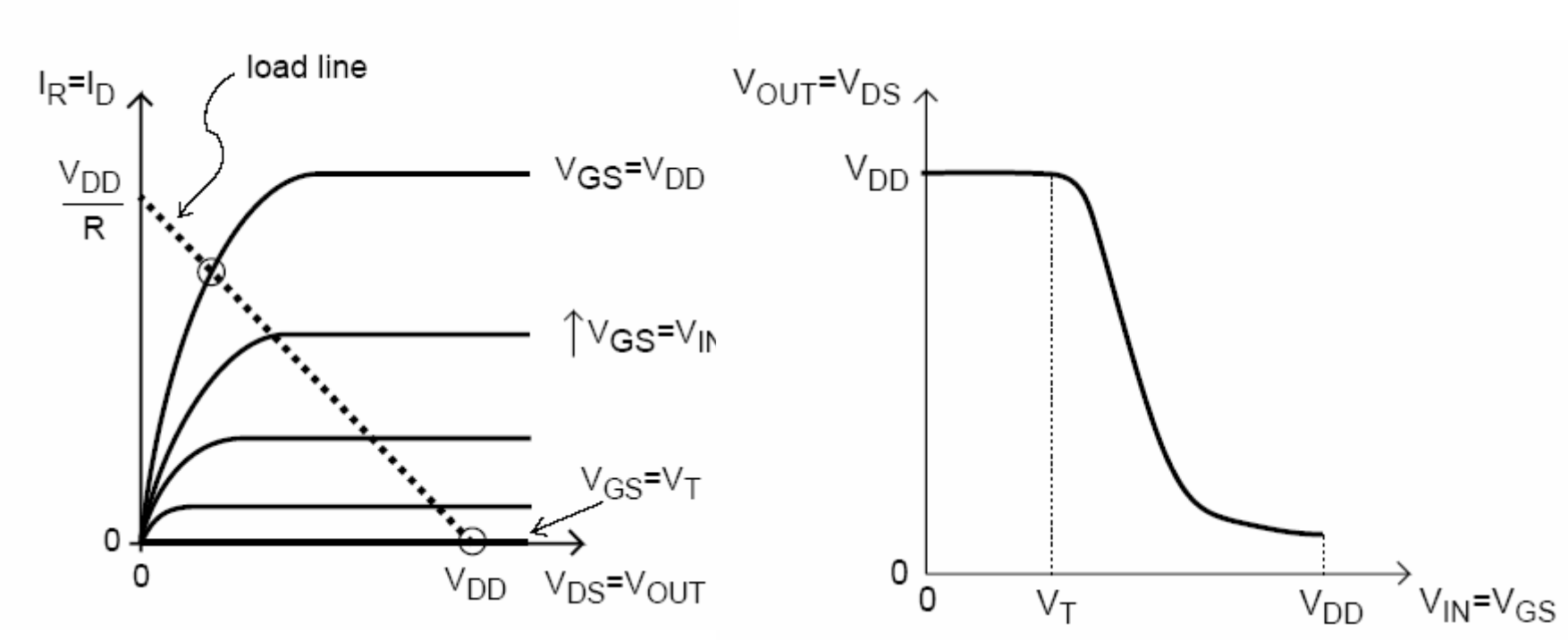
NMOS inverter with R:

Transfer Function using load-line analysis

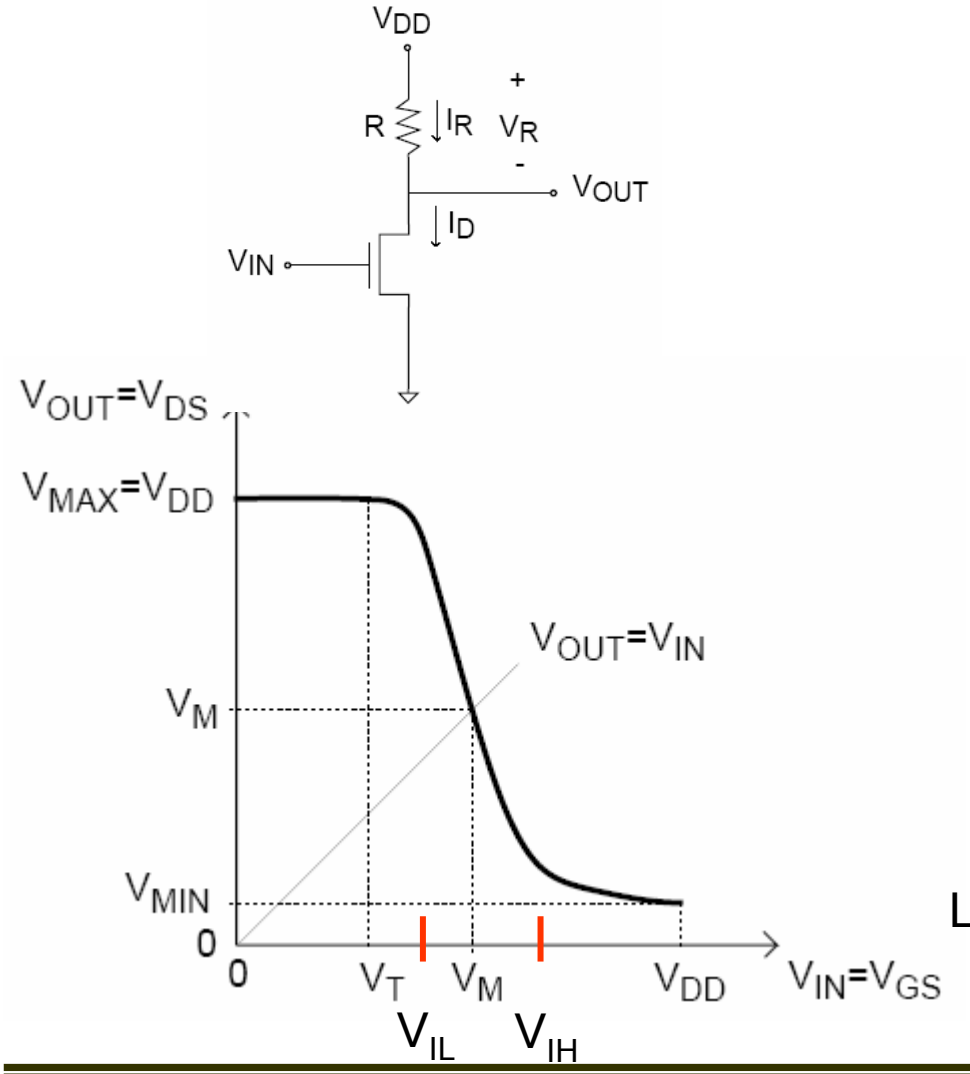




Lect. 20: Inverters



Lect. 20: Inverters



For V_{MIN},

$$I_D = \frac{W}{L}\mu_n C_{ox}(V_{DD} - \frac{V_{MIN}}{2} - V_T)V_{MIN}$$

$$= I_R = \frac{V_{DD} - V_{MIN}}{R}$$

For V_M,

$$I_D = \frac{W}{2L}\mu_n C_{ox}(V_M - V_T)^2$$

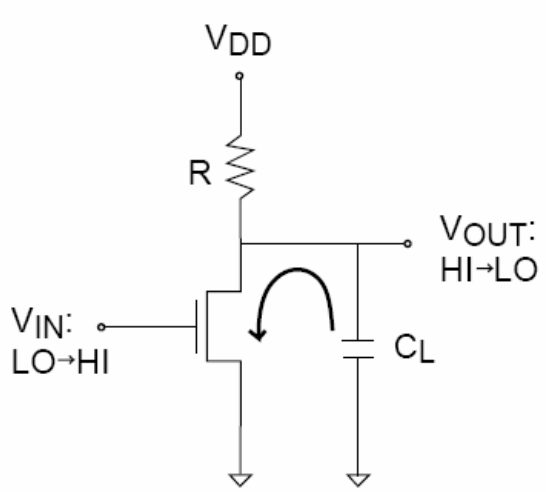
$$= I_R = \frac{V_{DD} - V_M}{R}$$

Larger Noise Margin ➔ Larger $|A_v|$

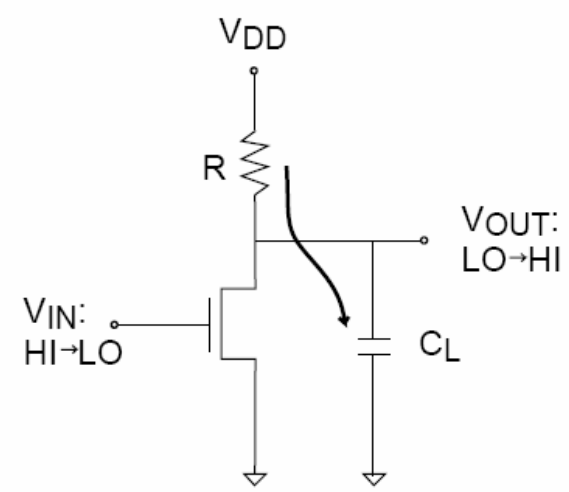
➔ Large g_m and R

Lect. 20: Inverters

Dynamics



pull-down



pull-up

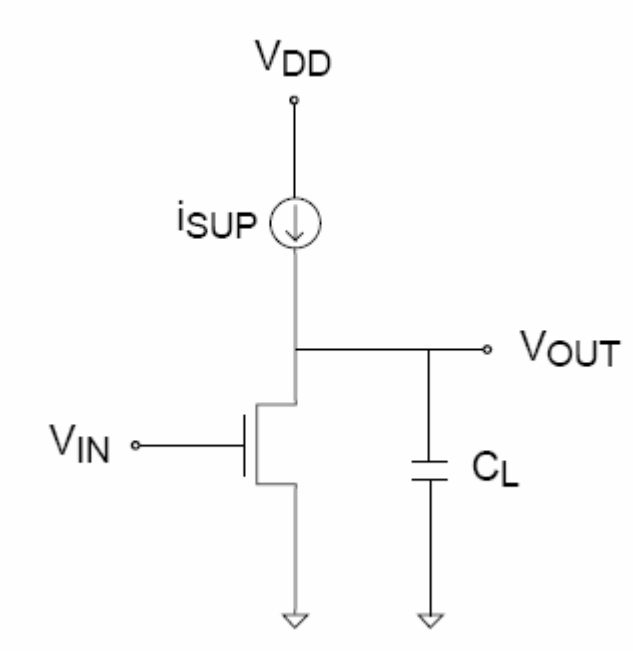
For faster operation: Small RC

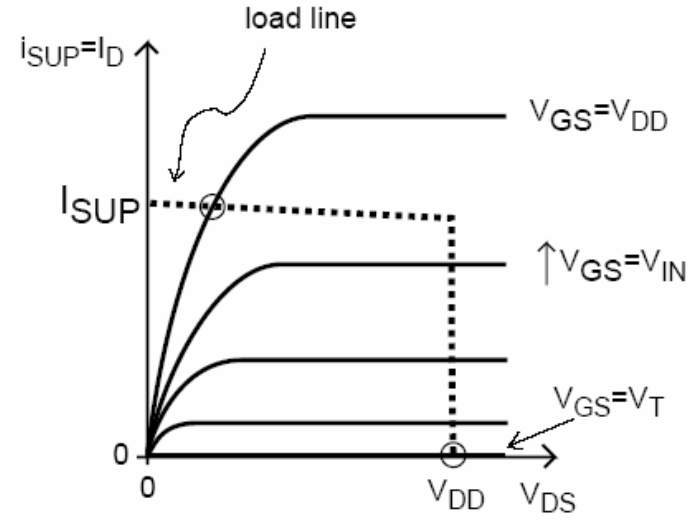
For large noise margin: Large $|A_v|$ ➔ Large R

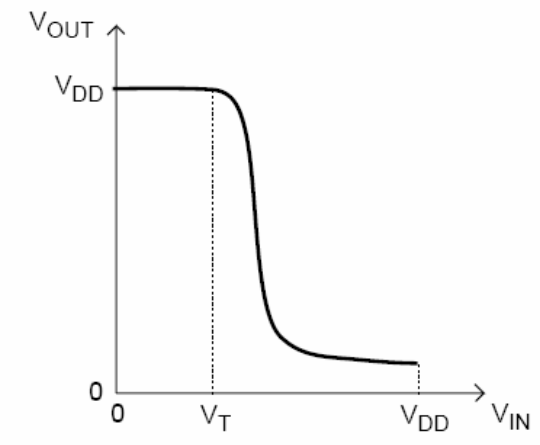
➔ Better way of implementing inverter?

Lect. 20: Inverters

Use current source instead of R

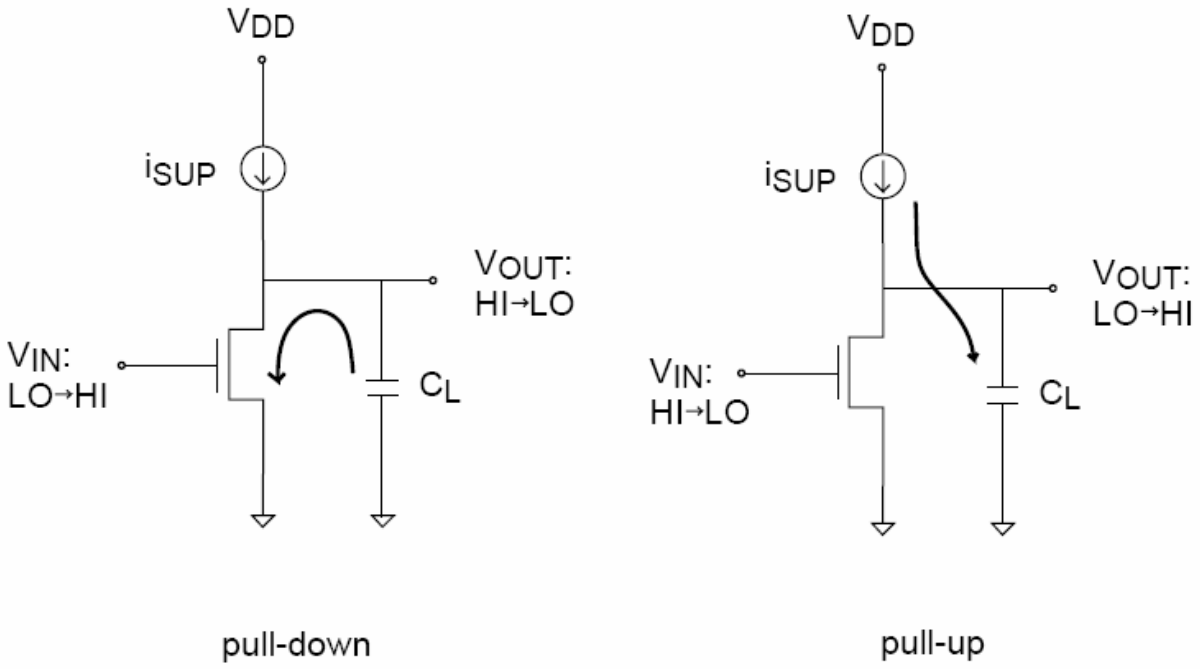






Lect. 20: Inverters

Dynamics:

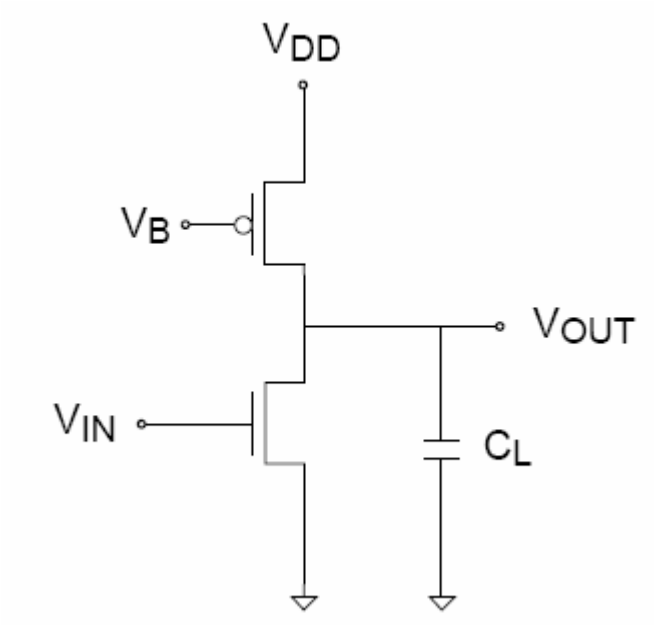


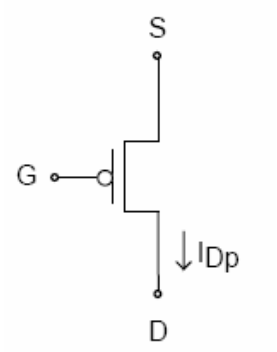
Faster pull-up because capacitor charged at constant current.

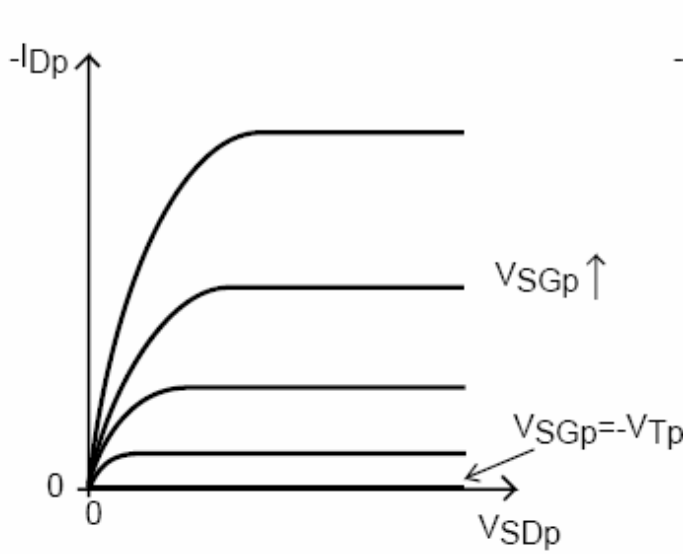
Lect. 20: Inverters

Simplest current source?

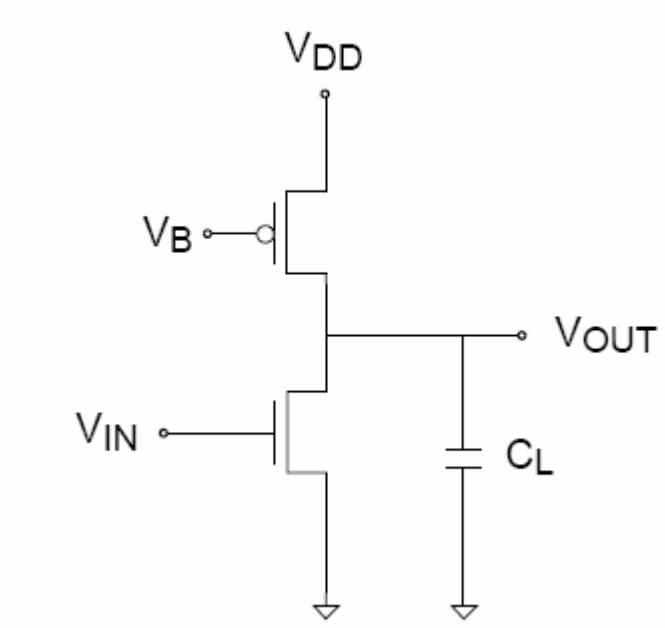
Use PMOS

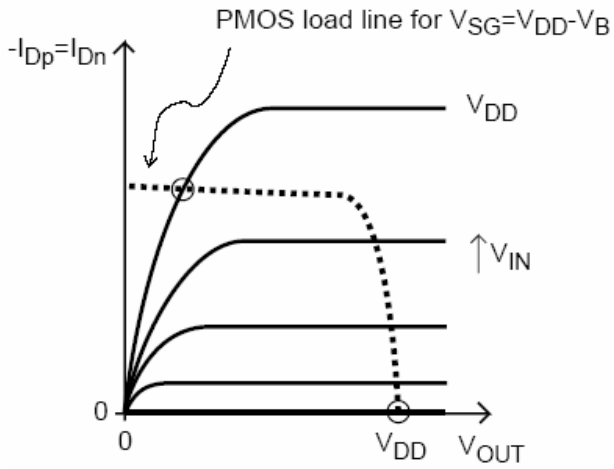




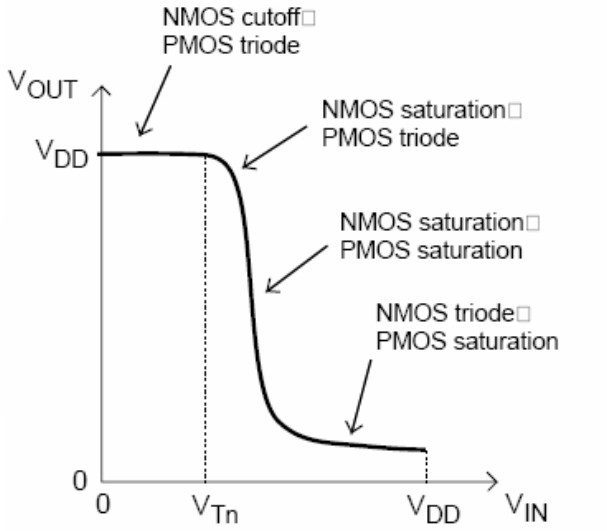


Lect. 20: Inverters





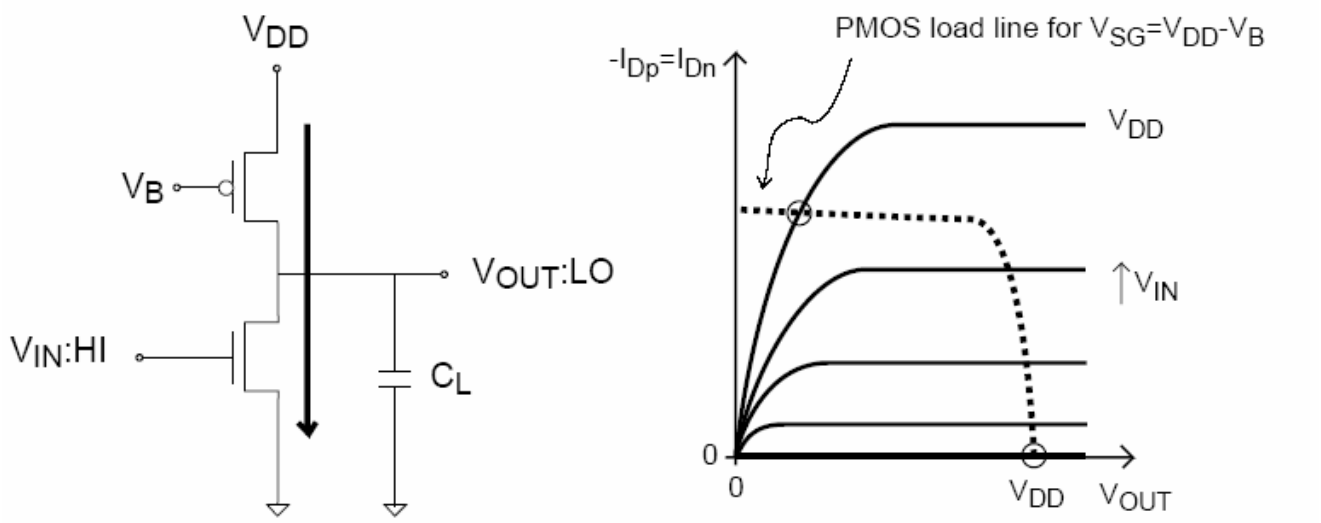
$$A_v = -g_{mn}(r_{on}//r_{op})$$



Lect. 20: Inverters

NMOS inverter with current-source pull-up allows fast switching with high noise margins.

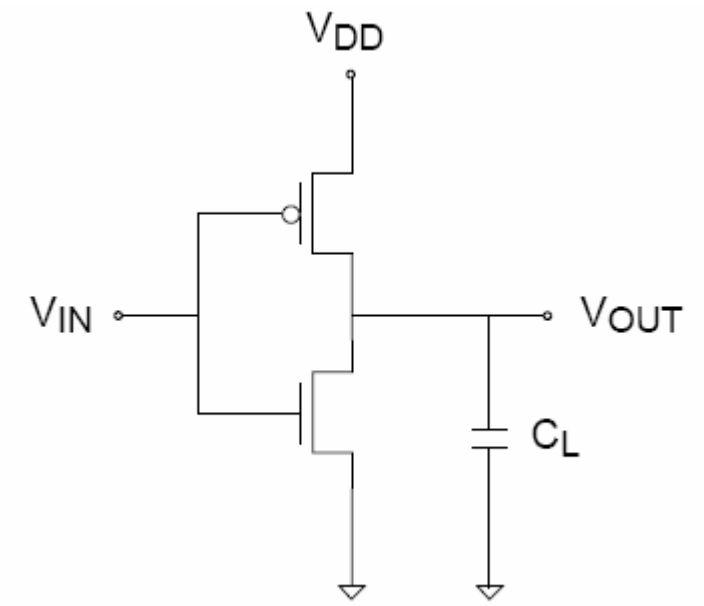
But... when $V_{IN} = V_{DD}$, there is a direct current path between supply and ground



Static Power consumption! ➔ How can we shut it off when input is high?

Lect. 20: Inverters

Complementary MOS (CMOS) Inverter



- $V_{IN} = 0 \Rightarrow V_{OUT} = V_{DD}$

  $V_{GSn} = 0 < V_{Tn} \Rightarrow$ NMOS OFF

  $V_{SGp} = V_{DD} > -V_{Tp} \Rightarrow$ PMOS ON

- $V_{IN} = V_{DD} \Rightarrow V_{OUT} = 0$

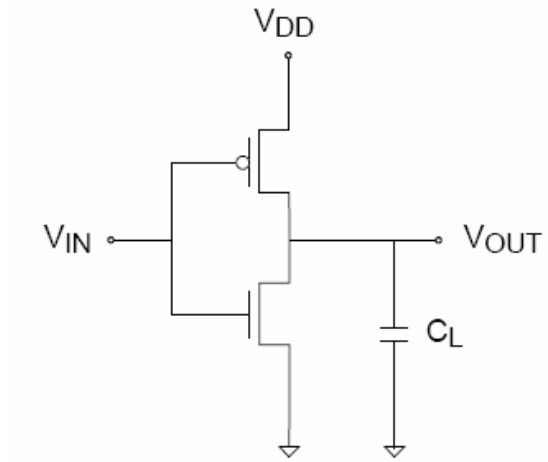
  $V_{GSn} = V_{DD} > V_{Tn} \Rightarrow$ NMOS ON

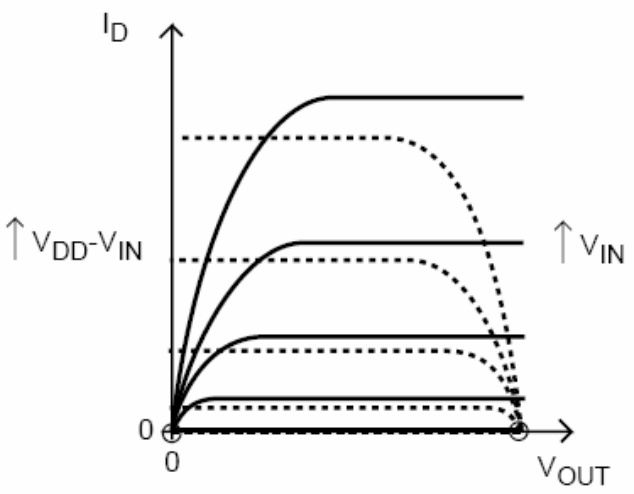
  $V_{SGp} = 0 < -V_{Tp} \Rightarrow$ PMOS OFF

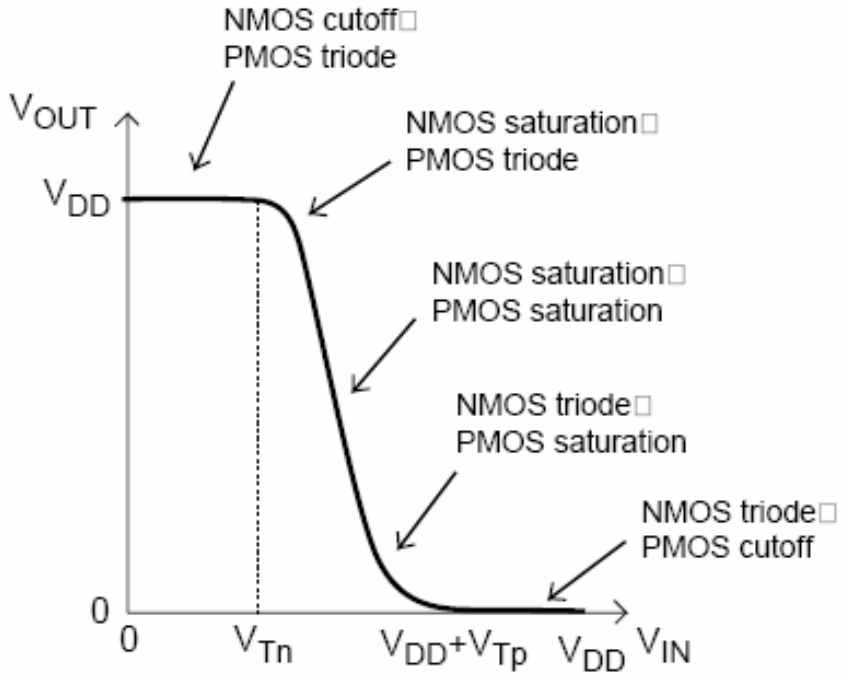
No power consumption while idling in any logic state.

➔ The most popular building block for today's digital electronics!

Lect. 20: Inverters



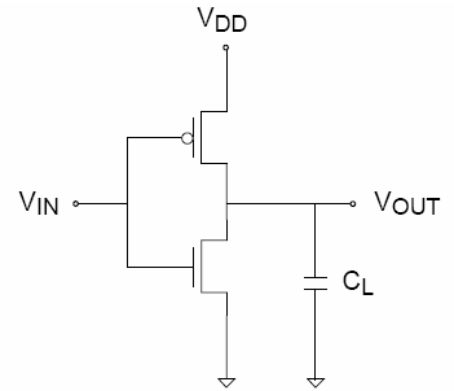


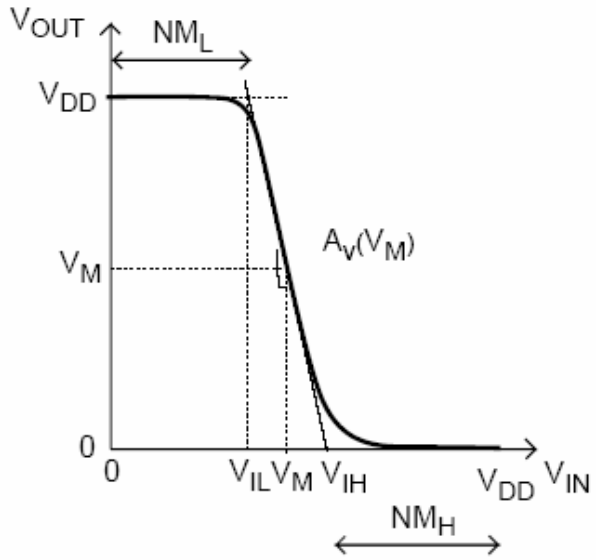


Rail-to-Rail logic

Lect. 20: Inverters

Estimation of important parameters for CMOS inverter: V_M, $A_v(V_M)$, NM_L, NM_H





For V_M ($V_{IN} = V_{OUT} = V_M$)

$$\frac{1}{2}\frac{W_n}{L_n}\mu_n C_{ox}(V_M - V_{Tn})^2 = \frac{1}{2}\frac{W_p}{L_p}\mu_p C_{ox}(V_{DD} - V_M + V_{Tp})^2$$

Using $$k_n = \frac{W_n}{L_n}\mu_n C_{ox}, \quad k_p = \frac{W_p}{L_p}\mu_p C_{ox}$$

$$V_M = \frac{V_{Tn} + \sqrt{\frac{k_p}{k_n}}(V_{DD} + V_{Tp})}{1 + \sqrt{\frac{k_p}{k_n}}}$$

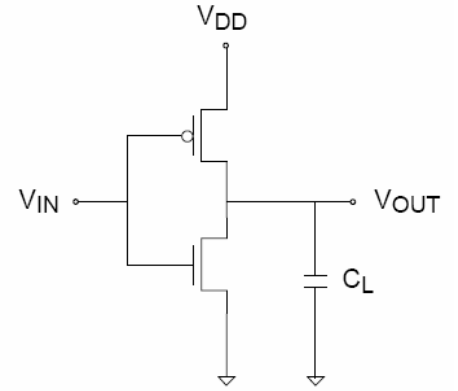
V_M can be engineered with controlling k_p/k_n

Assuming $V_{Tn}=-V_{Tp}$ and $k_p=k_n$, $V_M = V_{DD}/2$

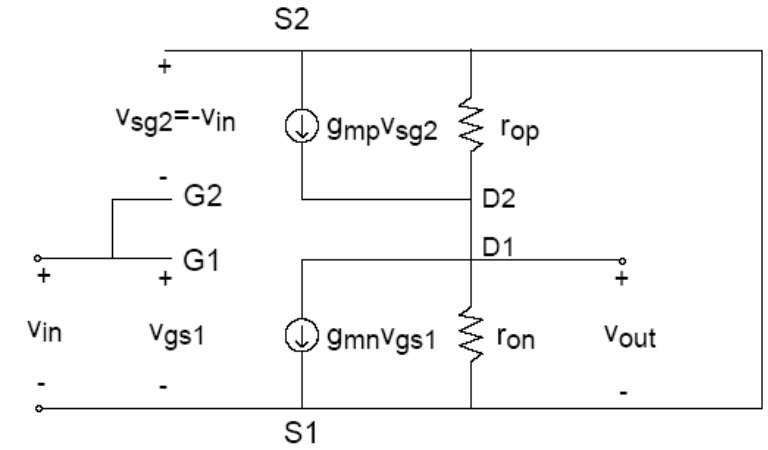
$$(W_p \simeq 3W_n)$$

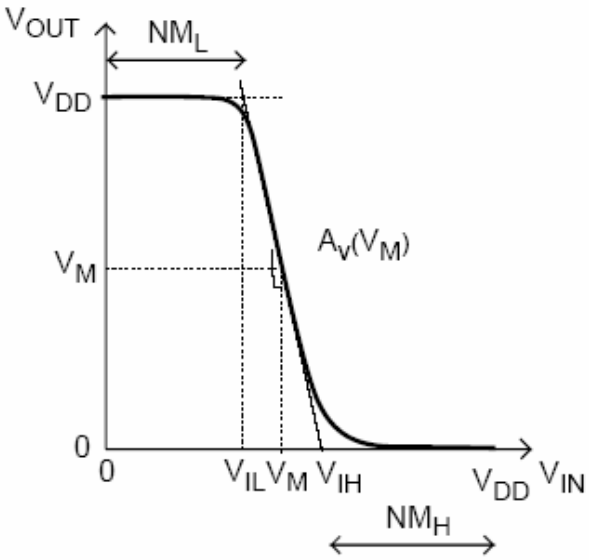
Lect. 20: Inverters

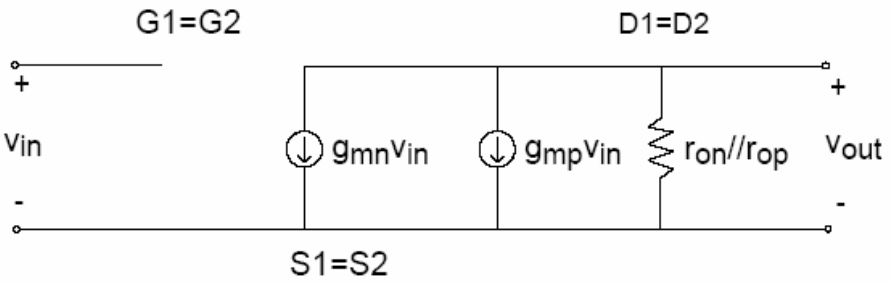
Estimation of important parameters for CMOS inverter: V_M, $A_v(V_M)$, NM_L, NM_H



$A_v(V_M)$



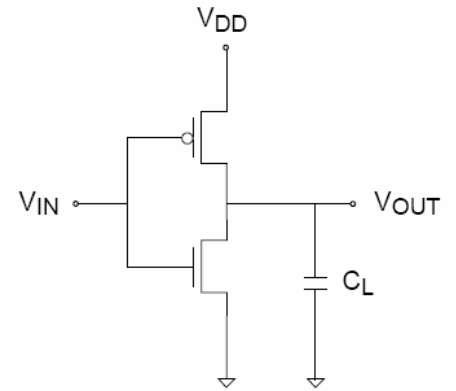


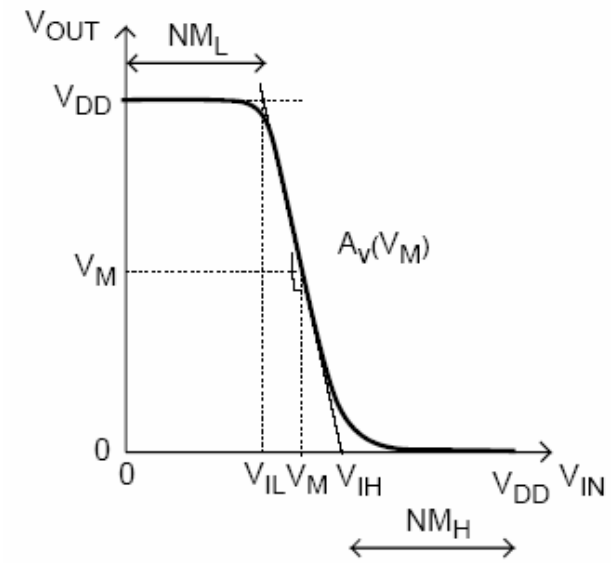


$$A_v = -(g_{mn} + g_{mp})(r_{on}//r_{op})$$

Lect. 20: Inverters

Estimation of important parameters for CMOS inverter: V_M, $A_v(V_M)$, NM_L, NM_H





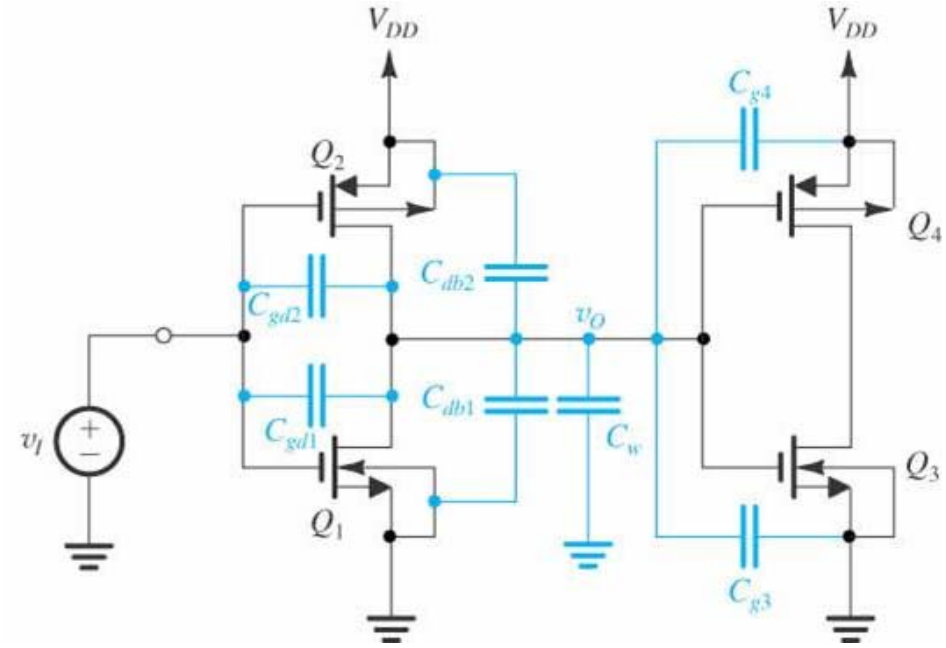
Noise Margins:

$N_{ML} = V_{IL} = V_M - \frac{V_{DD} - V_M}{|A_v|}$

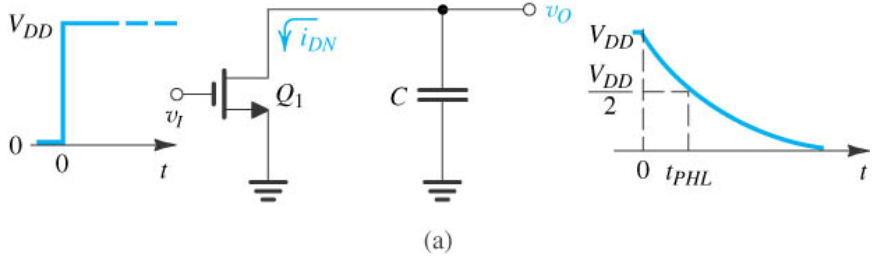
$N_{MH} = V_{DD} - V_{IH} = V_{DD} - V_M(1 + \frac{1}{|A_v|})$

Lect. 20: Inverters

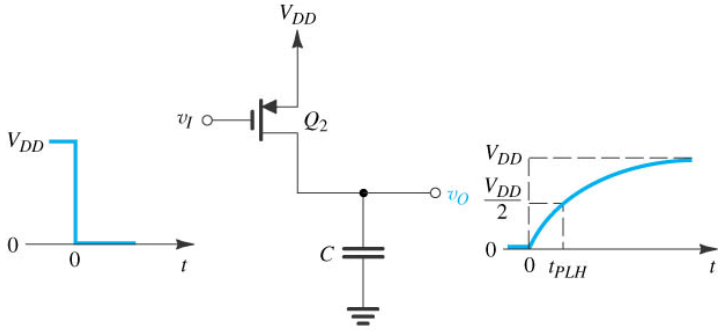
Estimation of propagation delay: Consider two inverters in a row



Model with
an equivalent capacitance C
Between v_O and ground



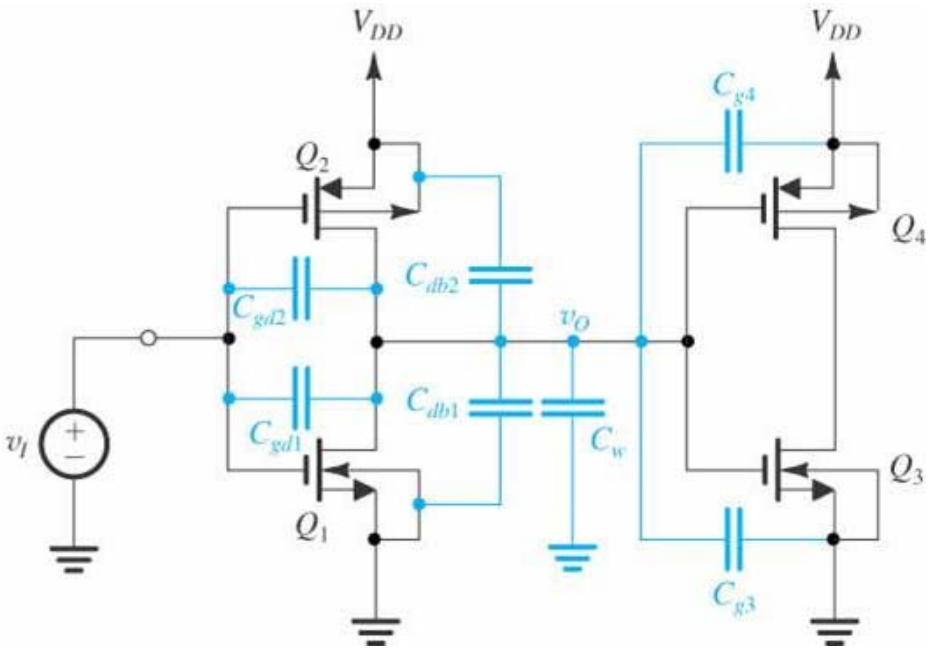
(a)



(b)

Lect. 20: Inverters

Estimation of propagation delay: Consider two inverters in a row

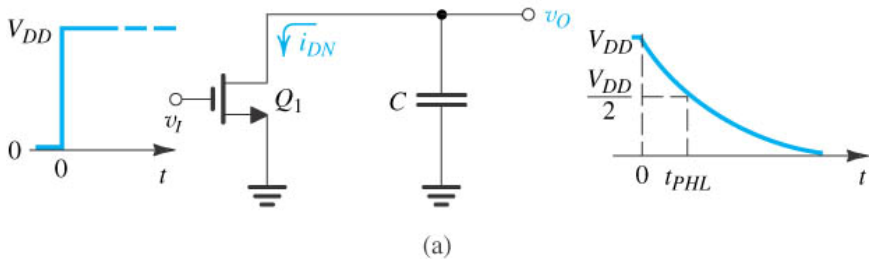


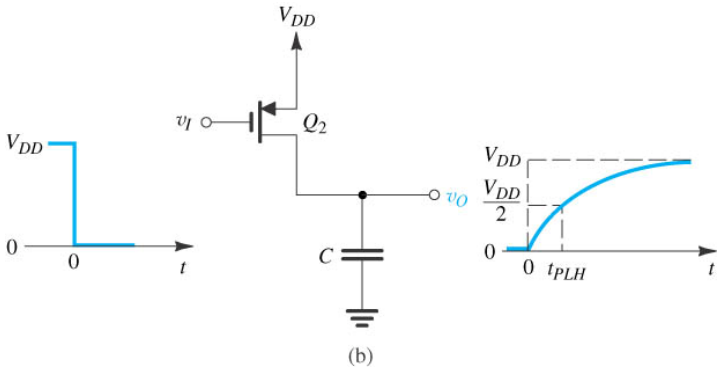
$$C = 2C_{gd1} + 2C_{gd2} + C_{db1} + C_{db2} + C_{g3} + C_{g4} + C_w$$

Factor of two for C_{gd} since voltage on both plates changes in the opposite direction

Lect. 20: Inverters

Estimation of propagation delay





$$t_{PHL} \simeq \frac{1.7C}{k_n'\left(\frac{W}{L}\right)_n V_{DD}}$$

$$t_{PHL} \simeq \frac{1.7C}{k_p'\left(\frac{W}{L}\right)_p V_{DD}}$$

$$t_P = \frac{1}{2}\left(t_{PHL} + t_{PLH}\right)$$

t_p goes down as V_{DD} goes up and L goes down

Each cycle Q = CV_{DD} is charged and discharged over V_{DD}

Dynamic power consumption: fCV_{DD}^2

➔ Make them smaller, smaller, smaller, smaller, smaller, smaller ...